A General Framework for SPICE-TLM Interconnection

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ABSTRACT — ***A general SPICE-TLM interconnection framework will be presented. The connection algorithm is based on the representation of the TLM network by equivalent Thévenin and/or Norton sources. The framework opens new and far-reaching possibilities for hybrid global microwave and high-speed digital circuit modeling in time domain because it integrates the extensive circuit and device models of SPICE into general three-dimensional field solutions in real time.***

Keywords — Time Domain Modeling, TLM method, lumped device embedding, distributed device embedding, nonlinear devices, active devices, hybrid TLM-SPICE connection.

I. INTRODUCTION

TLM models field equations in terms of transmission line networks [1]. Park *et al* [2] have investigated a number of techniques for embedding lumped and distributed devices in the TLM mesh. We have generalized these techniques based on the representation of the TLM network by equivalent Thévenin voltage and/or Norton current sources. The interconnection framework allows engineers to combine the extensive circuit and device modeling capability of SPICE with a field-based TLM engine in real time. Thus, it opens up new avenues for hybrid analysis for high frequency and digital circuit engineering. The new framework allows embedding of SPICE models into TLM, as well as embedding of TLM substructures into SPICE.

As mentioned in [2] to [5], lumped elements can be connected to a TLM mesh either at the nodes (center of the cells) or at the cell boundaries. The major difference between these two approaches lies in the treatment of voltage impulses incident on the device. Node implementation places the device at the center of a TLM cell; impulses scattered at the nodes depend on the incident impulses and the device characteristics. On the other hand, boundary implementation places the device at the location halfway between two nodes; the scattering at nodes is not affected, but the impulses reflected back into the nodes depend on the device characteristics. The two approaches give identical results as long as the device is truly lumped.

In many practical situations, the device to be modeled may occupy a volume that is comparable to or even exceeds the size of a single TLM cell, yet its dimensions remain small compared to the spatial wavelength. In other words, the device is distributed over several TLM cells but remains quasi-lumped from a field perspective. This calls for a distributed interconnection between device and field. The proposed interconnection framework allows for both quasi-lumped and distributed device embedding into the field space.

II. INTERCONNECTION FRAMEWORK

Figure 1 depicts two possible scenarios of a general TLM-SPICE interconnection. In one case, the TLM structure is much larger than the SPICE circuit. In the other case, the TLM structure occupies only a small portion of a larger SPICE circuit. In both cases, the SPICE circuit may consist of lumped and distributed elements. As shown in the figure, the SPICE circuits can only be coupled to the TLM network at well-defined ports. Hence, the problem of interconnecting them boils down to defining Thévenin and/or Norton equivalent sources for the TLM mesh. Since these two types of sources are equivalent, one of them is sufficient for driving the SPICE circuits. TLM and SPICE being both time-domain solvers, the internal resistance Z_{TLM} of the Thévenin source (see Figure 2) is determined exclusively by a combination of the characteristic impedances of the link lines connected to the ports of the SPICE circuit.

The instantaneous open-circuit voltage of the Thévenin source is found by combining the voltage impulses incident in these lines. At time $k\Delta t$, the open-circuited voltage of the source is:

$$ {}_kV_{TLM} = 2_kV^i \qquad (1) $$

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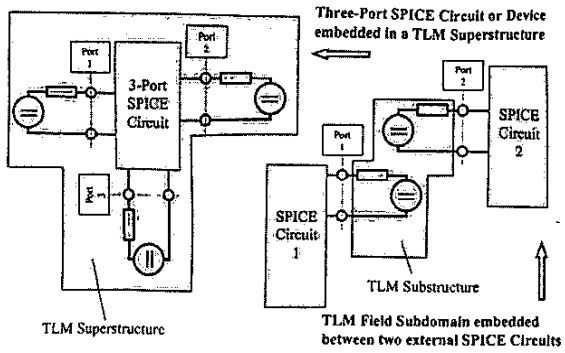

Figure 1 Interconnection between TLM and SPICE structures.

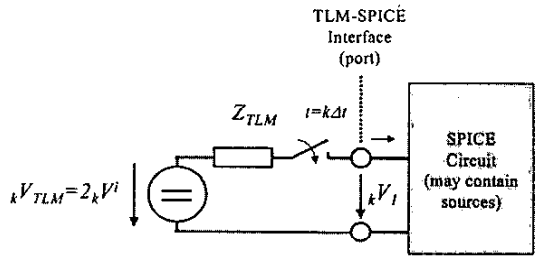

Figure 2 SPICE circuit driven by a Thévenin equivalent source that represents the TLM structure. The switch indicates that SPICE is working in the transient analysis mode.

where ${}_kV^i$ is a combination of all voltage impulses incident on the link lines coupled to the device. Figures 3 and 4 show two possible scenarios of coupling between a 3D TLM mesh and a two-terminal device. In Figure 3 a voltage-driven two-terminal SPICE device is represented by a cuboid volume sandwiched between two conducting surfaces. The TLM link lines polarized in the direction of the device voltage V_z form M stacks of N series-connected lines. The link lines polarized normal to V_z (not shown) are open-circuited on the device sidewalls. Assuming that all link lines have the same characteristic impedance, the total equivalent incident voltage is the average of the M stack voltages, and the equivalent TLM impedance is the shunt combination of the stack impedances:

$$
\begin{aligned}
{}_kV_{TLM} &= 2\,{}_kV^i = \tfrac{2}{M}\sum_m\sum_n {}_k v^i_{m,n} \\
Z_{TLM} &= \tfrac{1}{M}\sum_n Z_{m,n}
\end{aligned}
\qquad (2)
$$

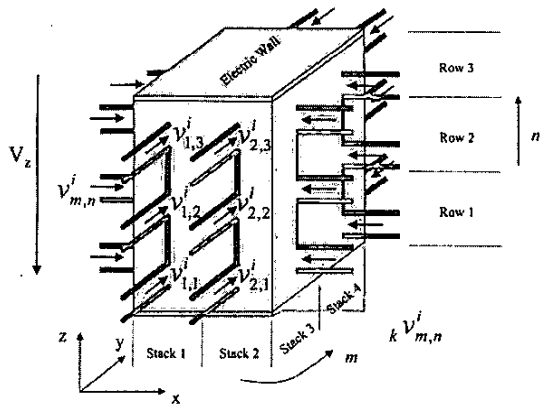

Figure 3 Stacks of TLM cells that lead to a Thévenin equivalent voltage source.

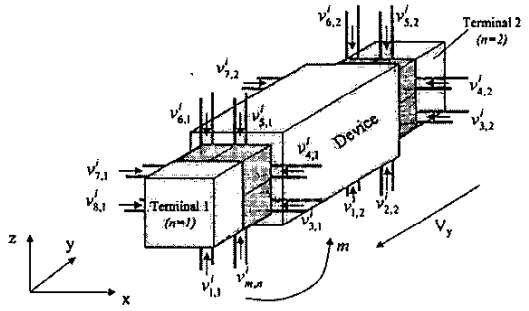

Figure 4 Blocks of TLM cells that lead to Norton equivalent current sources at the terminals.

For a current-driven SPICE circuit (Figure 4), instead of finding the Thévenin voltage sources we must obtain the Norton current sources. The procedure is a dual of the previous description. The TLM cells at the terminal interfaces constitute the loops of integration for finding the current entering and leaving the device terminals. Using the stack and row numbering convention shown in the above figures, the equivalent Thévenin voltage and impedance for terminal n with M pairs of link lines are:

$$
\begin{aligned}
{}_kV_{TLM} &= 2\,{}_kV^i = \tfrac{2}{M}\sum_m {}_k v^i_{m,n} \\
Z_{TLM} &= \tfrac{1}{M}\sum_m Z_{m,n}
\end{aligned}
\qquad (3)
$$

Once the equivalent the terminal voltage has been obtained, SPICE performs a transient analysis for the duration of one TLM time step. SPICE control statements allow the voltage and current states of reactive and nonlinear elements to be stored by the TLM solver who returns them to SPICE as initial conditions for the next

iteration. The TLM voltage impulses reflected from an interface port to TLM link lines are the difference between the total voltage computed by SPICE minus the incident voltage at the previous time step:

$$ {}_{k+1}V^{r}_{m,n} = {}_{k+1}V_{SPICE} - {}_{k}V^{i}_{m,n} \qquad (4) $$

Similar expressions can be derived for the current-driven representation in Figure 4. The interface ports must have a common ground for voltage and current sources. Furthermore, boundary conditions on the device surface must be enforced properly. The interface conditions at the device ports are automatically satisfied by the TLM impulses. The remaining facets must be replaced with magnetic or electric walls in the cases of voltage- or current-driven representation, respectively.

III. VALIDATION

We have tested the above interconnection framework with MEFiSTo, [6], and a public domain version of SPICE from Berkeley, [7]. The following examples demonstrate the power of this general interconnection framework. Note that the TLM part is kept as simple as possible without loss of generality. This enables us to compare the hybrid TLM-SPICE combination to a pure SPICE representation. Figure 5 depicts a parallel plate transmission line with a SPICE element at the center of the first transmission line. The second line is used as a reference to show the amplitude of the incident input signal. The lines are discretized with a $3\Delta l \times 3\Delta l \times 40\Delta l$ mesh, Δl=1mm. Figure 6 depicts the standing wave pattern as well as the time responses at the output nodes created by the SPICE network. The PSPICE analysis result in Figure 7 is in excellent agreement with the TLM-SPICE result in Figure 6. The resistor network in Figure 5 can be replaced with more complicated active elements. Figure 8 depicts the responses of a diode and a BJT network excited by a ramped sinusoidal excitation.

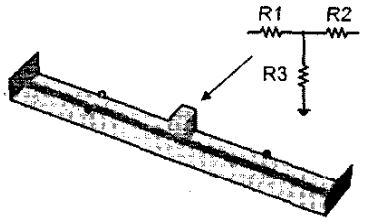

Figure 5 Two 377Ω parallel plate transmission lines. A T-network is inserted at the center of the first line. R1=R2=0, R3=377Ω. A 5V 8GHz sinusoidal TLM source is used to drive the structure.

Figure 9 shows the response of a common emitter amplifier excited by a 2GHz sinusoidal TLM signal. Identical response has been obtained with an equivalent PSPICE analysis, Figure 10.

IV. CONCLUSION

A general TLM-SPICE interconnection framework has been developed. This framework allows TLM and SPICE to couple field and circuit analysis in the time-domain. Such a combination has great potential for global microwave and high-speed and/or digital circuit modeling.

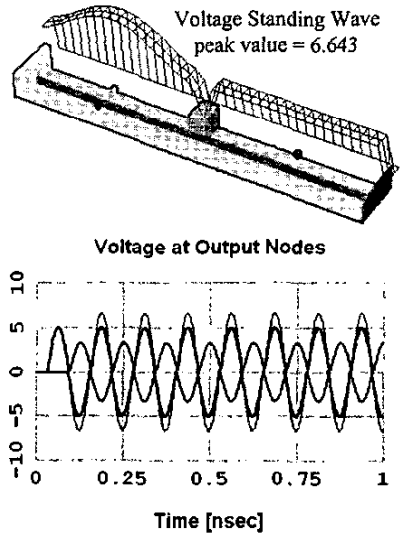

Figure 6 Standing wave pattern and time domain response.

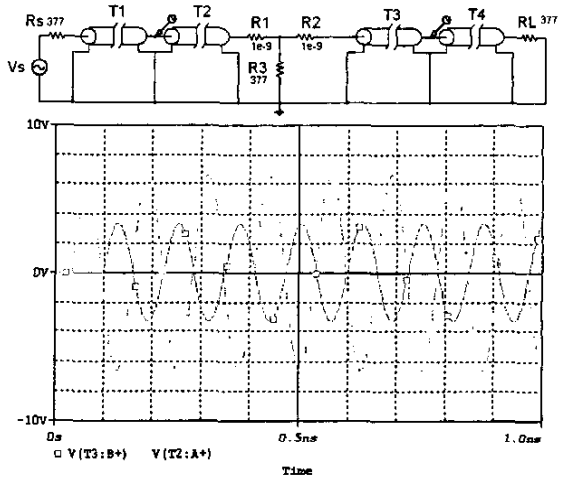

Figure 7 PSPICE schematic and analysis equivalent to the parallel plate structure in Figure 5. The Thévenin equivalent source, Vs, has 10V amplitude; T2 has a delay of 32.5ps.

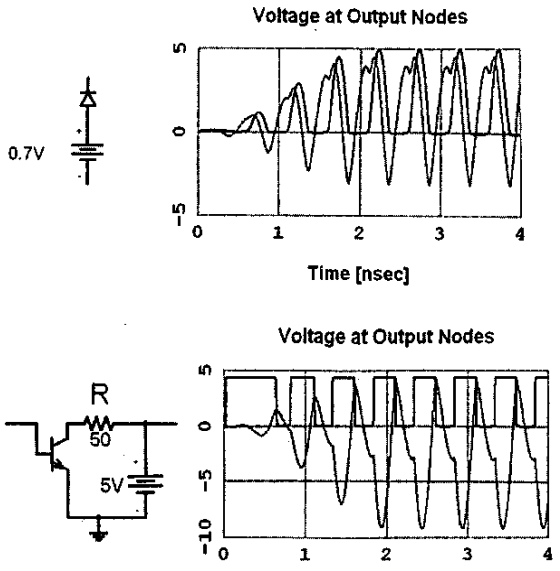

Figure 8 The responses of a diode and a BJT circuit insert in the parallel plate structure in Figure 5. The TLM excitation source is a 5V 2GHz sinusoidal signal.

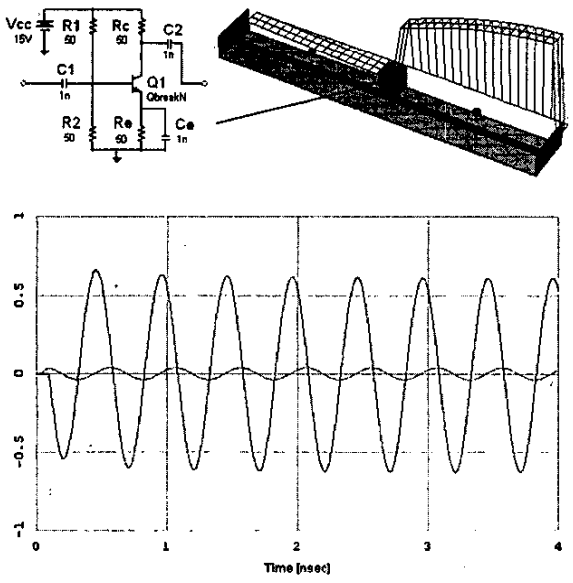

Figure 9 A common emitter amplifier SPICE circuit driven by a 0.05V 2GHz sinusoidal TLM source. Amplification can be clearly observed from the voltage distribution in both space and time domains.

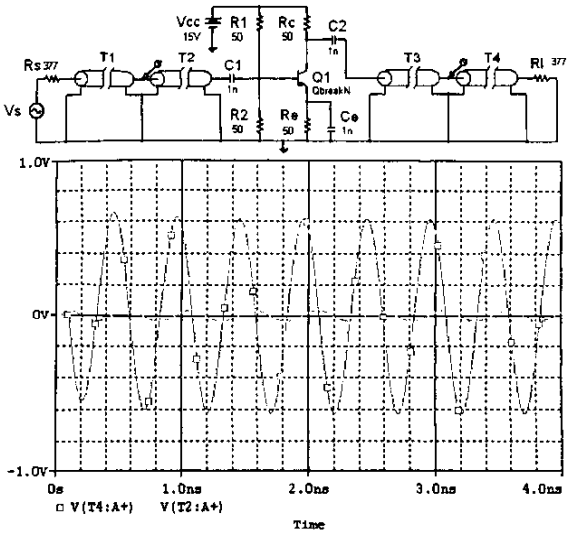

Figure 10 PSPICE schematic and its response. The Thévenin equivalent source has 0.1V amplitude; T2 has a delay of 32.5ps.

V. REFERENCES

[1] P. B. Johns, ***A symmetrical condensed node for the TLM method***, IEEE Trans. Microwave Theory Tech., vol. 35, pp. 370-377, Apr. 1987.

[2] J.W. Park, P.P.M. So and W.J.R. Hoefer, ***Lumped and Distributed Device Embedding Techniques in Time Domain TLM Field Models***, IEEE MTT-S Digest, June 2001.

[3] P. Russer, P. P. M. So, and W. J. R. Hoefer, ***Modeling of nonlinear active regions in TLM***, IEEE Microwave Guided Wave Letter, vol. 1, pp. 10-13, Jan. 1991.

[4] P. Russer, M. Righi, C. Eswarappa, and W. Hoefer, ***Lumped element equivalent circuit parameter extraction of distributed microwave circuits via TLM simulation***, in IEEE MTT-S Digest, pp. 887-890, 1994.

[5] L. Cascio, G. Tardioli, and W. Hoefer, ***Modeling of nonlinear active and passive devices in three dimensional TLM networks***, in IEEE MTT-S Digest, pp. 383-386, 1997.

[6] MEFiSTo, Faustus Scientific Corporation.

[7] SPICE, University of California, Berkeley.

[8] PSPICE, Cadence Design Systems.